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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,784	03/22/1999	JOHN G. MCBRIDE	10971308-1	7570

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/273,784	MCBRIDE, JOHN G.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- *Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.*
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- *If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.*
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,9,15 and 16* is/are rejected.

7)☒ Claim(s) *3-7,10-14 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on 05/17/2004. Claims 1- 20 are pending in this Action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 8, 9, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hall, David, US patent no. 5,936,868.

As per claims 1 and 15, Hall discloses a method and system for estimating design performances, including handling cross-coupling effects, simultaneous switching, etc. for device characterization including noise analysis or noise immunity with feature limitations similar to the claimed invention (Summary of the Invention, page 5, lines 18-26, for example). According to Hall, the rule checking method and system for design rule verification includes means such as

A computer configured to execute a rule checker program (Field of the invention and Background of the Invention, col. 6, lines 55-58, for the system specification and implementation), wherein the design rule being checked for noise performance of an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths,

lengths, connected in device channel, etc. ("Summary of the Invention", col. 7, line 21 to col. 8, line 25, for instance). The design rule checker program is to check transistor noises such as transient noise, noise levels, etc. (col. 7, line 35 to col. 8, line 26, for example). Hall discloses steps of analyzing the widths of gate channel to determine noise generated in MOSFET (see col. 7, equation 3, the numerator and denominator of equation 3). This equation shows noise generated in the MOS transistor including the new MOS version of the upgraded IC. In other words, the noise equation in col. 7 shows acceptable and allowable noise levels for the integrated circuit design. Hall does not expressly disclose noise immunity in the design rule checking as claimed.

Practitioner in the art at the time of the invention was made would have found Hall disclosure of design rule checking for checking acceptable noise level or allowable noise as above implies the feature of noise immunity as claimed such that circuit under operation is immune to noise, or certain allowable noise levels.

As per claim 2, Hall discloses transistor design parameters and reading design parameters such as transistor channel length, gate width, channel widths, and the likes for checking design rule as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design, and the rule checking of the gate circuit statically verifies device characteristics and performance analysis such as susceptibility for noise levels, acceptable transient noise in a specified design operation bound within thresholds

values as known in MOS and CMOS of the circuit design (col. 7, line 34 to col. 8, line 26).

As per claim 8, Hall discloses a method and system for estimating design performances, including handling cross-coupling effects, simultaneous switching, etc. for device characterization including noise analysis or noise immunity with feature limitations similar to the claimed invention (Summary of the Invention, page 5, lines 18-26, for example). According to Hall, the rule checking method and system for design rule verification includes means such as

A computer configured to execute a rule checker program (Field of the invention and Background of the Invention, col. 6, lines 55-58, col. 10, lines 19-34, for the system specification and implementation), wherein the design rule being checked for noise performance of an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", col. 7, line 35 to col. 8, line 25, for instance). The design rule checker program is to check transistor noises such as transient noise, noise levels, etc. (col. 7, line 35 to col. 8, line 26, for example). Hall discloses steps of analyzing the widths of gate channel to determine noise generated in MOSFET (see col. 7, equation 3, the numerator and denominator of equation 3). This equation shows noise generated in the MOS transistor including the new MOS version of the upgraded IC. In other words, the noise equation in col. 7 shows acceptable and allowable noise levels for the integrated

circuit design. Hall does not expressly disclose noise immunity in the design rule checking as claimed.

Practitioner in the art at the time of the invention was made would have found Hall disclosure of design rule checking for checking acceptable noise level or allowable noise as above would imply the feature of noise immunity as claimed such that circuit under operation is acceptable for certain noise levels or immune to noises, or certain noise generated are allowable for the MOS field effect transistor under operation.

As per claim 9, Hall discloses transistor design parameters and reading design parameters such as transistor channel length, gate width, channel widths, and the likes for checking design rule as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design, and the rule checking of the gate circuit statically verifies device characteristics and performance analysis such as susceptibility for noise levels, acceptable transient noise in a specified design operation bound within thresholds values as known in MOS and CMOS of the circuit design (col. 7, line 34 to col. 8, line 26).

As per claim 16, Hall discloses transistor design parameters and reading design parameters such as transistor channel length, gate width, channel widths, and the likes for checking design rule as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in

transistor circuit design, and the rule checking of the gate circuit statically verifies device characteristics and performance analysis such as susceptibility for noise levels, acceptable transient noise in a specified design operation bound within thresholds values as known in MOS and CMOS of the circuit design (col. 7, line 34 to col. 8, line 26).

Allowable Subject Matter

1. Claims 3-7, 10-14, and 17-20 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent forms including all of the limitations of the base claims and any intervening claims.

2. Dependent claims 3-7, 10-14, and 17-20 are objected to because the claims require a plurality of checking models for rule checking program and method, each rule checking model is associated with ratio of the width of the P-field transistor to the width of the N-field transistor, the ratio corresponding to the numerical value stored in the memory device. In each checking model, the rule checker program obtaining a (first) ratio of the width of the n and p-type transistor of the first model, the first ratio used to access the first and second threshold values stored in the memory device, the rule checker program determines noise levels on the inputs taking possible high or low values, and compares the determined noise levels to the first and second threshold values to determine the gate meets acceptable noise immunity requirement with respect to each model as claimed herein. The closest prior art of record does not expressly disclose such limitations as in the dependent claims.

Response to Arguments

1. Applicant's arguments filed 05/10/2004 have been fully considered but they are not persuasive.

2. In response to applicant's argument Hall does not expressly disclose or suggest method for analyzing the widths of the field effect CMOS transistors to determine the gate noise immunity (pages 16-17), the examiner disagrees with. Hall discloses steps of analyzing the widths of gate channel to determine noise generated in MOSFET (see col. 7, equation 3, the numerator and denominator of equation 3). This equation shows noise generated in the MOS transistor including the new MOS version of the upgraded IC. In other words, the noise equation in col. 7 shows acceptable and allowable noise levels for the integrated circuit design.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US patent no. 4,806,801, issued to Argade et al, on Feb. 1989

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 703-305-3812. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 703-308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aug. 27, 2004

Thai Phan
Patent Examiner
Art Unit 2128